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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte TZU-HUNG LIN and
THOMAS MATTHEW GREGORICH

Appeal 2015-007559
Application 13/753,537
Technology Center 2800

Before TERRY J. OWENS, KAREN M. HASTINGS, and
MONTÉ T. SQUIRE, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

The Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1–20. We have jurisdiction under 35 U.S.C. § 6(b).

The Invention

The Appellants claim a flip chip package. Claim 1 is illustrative:

1. A flip chip package, comprising:
a substrate having a die attach surface; and
a die mounted on the die attach surface with an active surface of the die facing the substrate, wherein the die is interconnected to the substrate through a plurality of copper pillar bumps on the active surface, wherein at least one of the plurality of copper pillar bumps has a bump width that is substantially equal to or smaller than

> a line width of a trace on the die attach surface of the substrate, and wherein the at least one of the plurality of copper pillar bumps is directly jointed to the trace.

The References

Tan	US 2005/0077624 A1	Apr. 14, 2005
Salmon	US 2006/0079009 A1	Apr. 13, 2006
Cheng	US 2011/0101527 A1	May 5, 2011

The Rejections

The claims stand rejected as follows: claims 1, 11–14 and 20 under 35 U.S.C. § 102(b) over Salmon; claims 2, 8–10 and 15 under 35 U.S.C. § 103 over Salmon; claims 3 and 16 under 35 U.S.C. § 103 over Salmon in view of Tan; and claims 4–7 and 17–19 under 35 U.S.C. § 103 over Salmon in view of Cheng.

OPINION

We reverse the rejections. We need address only the independent claims (1 and 14).[1] Claim 1 requires a flip chip package comprising a trace on a substrate's die attach surface, and a die having on its active surface a plurality of copper pillar bumps, at least one of which is directly joined to the trace. Claim 14 requires a flip chip package comprising a trace on a substrate's die attach surface, and a die having on its active surface a plurality of copper pillar bumps which interconnect the die to the substrate, wherein no substrate via is interposed between at least one of a plurality of copper pillar bumps and the trace.

[1] In the rejections under 35 U.S.C. § 103 the Examiner does not apply any obviousness rationale regarding the independent claims' limitations or rely upon Tan or Cheng for any disclosure that remedies the deficiency in Salmon as to the independent claims (Final Act. 4–9).

An examiner has the initial burden of establishing a prima facie case of anticipation by pointing out where all of the claim limitations appear in a single reference. *See In re Spada*, 911 F.2d 705, 708 (Fed. Cir. 1990); *In re King*, 801 F.2d 1324, 1327 (Fed. Cir. 1986).

Salmon discloses a flip chip package comprising 1) an interconnection substrate (19) having on its die attach surface a thick layer of dielectric (25) with conductive layer (26)-coated wells (24) therein, 2) a semiconductor chip (5), and 3) a plurality of copper mesas (4) (which are a form of a bump), each attached at one of its ends to the semiconductor chip (5)'s active surface and temporarily or permanently at the other of its ends to an electrically conductive fluid or paste in one of the wells (24) (¶¶ 17–19; Fig. 2). One of the wells (24) (numbered 29 in Fig. 2) is electrically connected to a trace (28) by way of the well (24)'s electrically conductive layer (26) and a via (27) in the interconnection substrate (19) (¶ 18).

The Examiner finds that the Appellants' disclosed copper pillar bump (310a, 310b)'s copper layer (312) is not directly joined to a trace (210a, 210b) but, rather, is joined through an intermediate part (solder cap 314) (Spec. ¶ 24; Fig. 3), and that "Salmon's copper pillar bumps 4 are directly joined to the Salmon's trace 28 [sic] through the intermediate part (24, 26, and 27)" (Ans. 4).[2]

The Appellants' claim 1 requires that the copper pillar bump, not the copper pillar bump's copper layer, is directly joined to the trace. The Appellants' copper pillar bump (310a, 310b), which includes the copper layer (312) and the solder cap (314), and is directly joined to the trace (210a,

[2] An optional under bump metallurgy (UBM) layer (311) is on the side of the copper layer (312) opposite to the solder cap (314) (¶¶ 24, 29; Fig. 5).

210b) (¶ 24; Fig. 3). Thus, the Examiner errs in concluding that the Appellants' claim 1's term "directly joined" encompasses Salmon's joining of the semiconductor chip (5) to the trace (28) by way of a well (24), a conductive layer (26) and a via (27) (Fig. 2).

Relevant to claims 1 and 14, the Examiner finds, based upon glossary definitions of "trace" and "route", that a trace is a "[s]egment of a route"[3] and a route is "[a] layout or wiring of a connection",[4] and that Salmon's well (24) is conductive and is a segment of a connection (interconnection circuit 22) and, therefore, is a trace (Ans. 4–7).

The glossary relied upon by the Examiner states that "[t]he words have other meanings not given here."[5] "'[D]uring examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification.'" *In re Translogic Tech. Inc.*, 504 F.3d 1249, 1256 (Fed. Cir. 2007) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). The Appellants' Specification describes (¶ 7) and illustrates (Figs. 2, 3), a trace as a flip chip package substrate lead. That indication of the meaning of "trace" is consistent with definition of that term in other sources ("A path made of copper on a PCB [printed circuit board]. It is used in the same manner as electrical wires, to connect the components of a board."[6]; "a continuous path of copper on a circuit board"[7]). The Examiner does not

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[3] Golden Gate Graphics, *Glossary of Printed Circuit Design and Manufacturing*, *at* http://goldengategraphics.com/pcgloss.htm#trace.
[4] *Id. at* http://goldengategraphics.com/pcgloss.htm#route.
[5] *Id*. at first page.
[6] PCB Terminology 101, *at* http://www.build-electronic-circuits.com/pcb-terminology/.
[7] PCB Basics, *at* https/learn.sparkfun.com/tutorials/pcb-basics/terminology.

address the Appellants' disclosure and establish that the broadest reasonable interpretation of the Appellants' claim term "trace" consistent with that disclosure includes Salmon's well (24).

Accordingly, we reverse the rejections.

DECISION/ORDER

The rejections of claims 1, 11–14 and 20 under 35 U.S.C. § 102(b) over Salmon, claims 2, 8–10 and 15 under 35 U.S.C. § 103 over Salmon, claims 3 and 16 under 35 U.S.C. § 103 over Salmon in view of Tan and claims 4–7 and 17–19 under 35 U.S.C. § 103 over Salmon in view of Cheng are reversed.

It is ordered that the Examiner's decision is reversed.

REVERSED